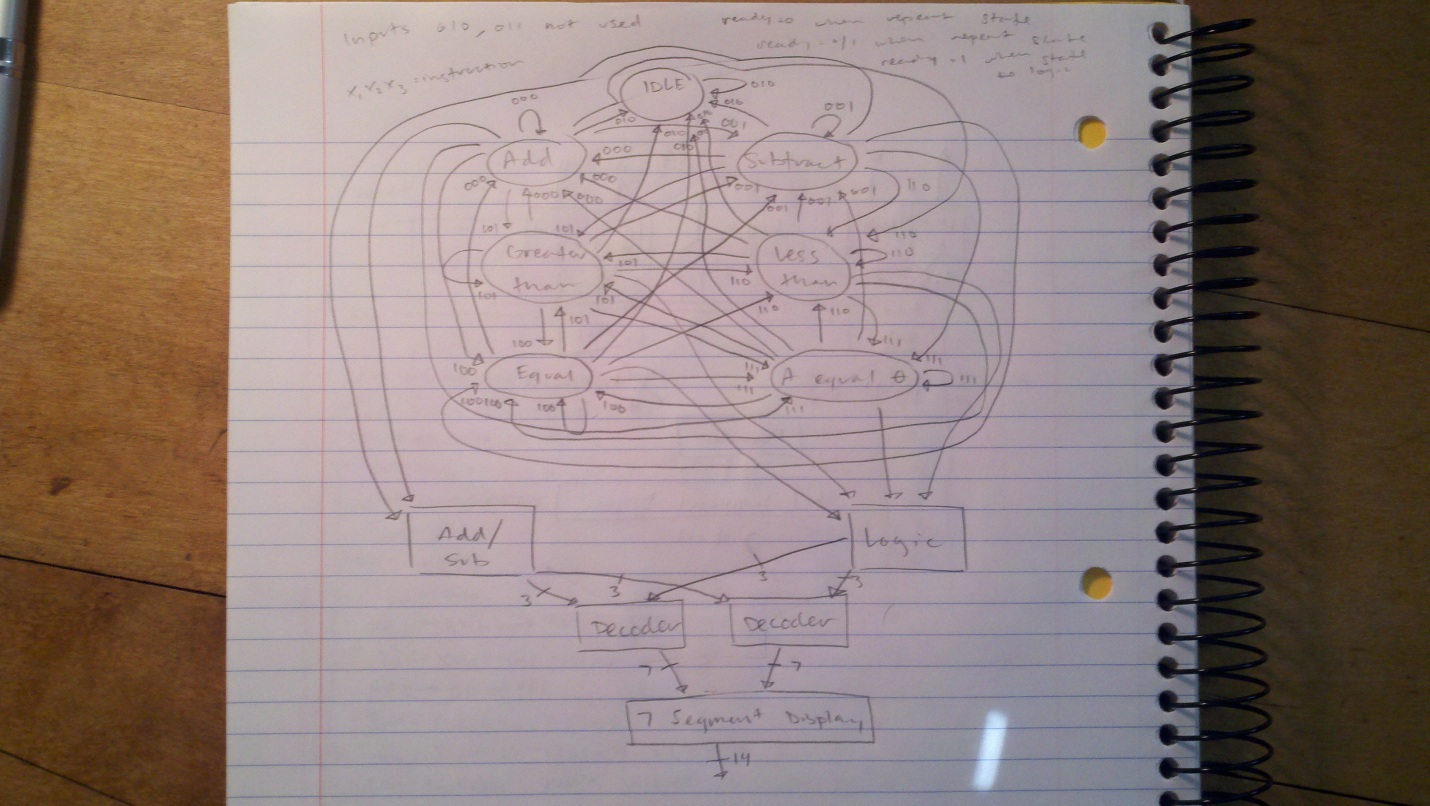
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EPCE 174

**Pre-Lab #6A**

ALU Block Diagram:



In the block diagram of the ALU above, the logic “Add/Sub” and “Logic” is used as datapath, while the finite state machine is control. This is because as the user has control over the system, that logic will be defined as control. Otherwise, if the system handles the information internally, this is datapath.

Design/Implementation/Test:

In order to design, implement, and test the ALU, we will begin by writing VHDL. We have already begun writing our code, of course after designing our block diagram. Our code includes separate VHDL files for the adder/subtractor, logic, FSM, and of course the seven segment display. As of now, we plan to display our output in base 10, or decimal. Although this creates an additional step to convert binary to decimal, the extra initial effort is worth it, so we don’t have to convert our answers during testing. I’m not exactly sure why this section needs to be extensive, as the process in designing our ALU is not complex. Multiple VHDL files will be used, and ported into our VHDL main. For each VHDL that is not working properly, that specific file will be debugged. Once all our files are working in conjunction and as desired, we will import our design onto the FPGA board. If errors arise in this process, our first check will be if pin assignments are assigned correctly. If this is not the case, further debugging measures will be taken.

VHDL:

See attached.